life.augmented

PRODUCT / PROCESS CHANGE NOTIFICATION

ST Ang Mo Kio (Singapore) additional wafer fab for industrial grade EEPROM products manufactured with CMOSF8H+ technology

What is the change?
The CMOSF8H+ process technology running in ST Rousset (France) 8 inch fab (R8) has been also qualified in ST Singapore 8 inch fab (SG8E) for double source wafer manufacturing.

The M24128, M24C16, M24C04, M24C02 industrial grade EEPROM currently produced with CMOSF8H+ process technology in ST Rousset 8 inch Fab (R8), will be also produced with same process technology in ST Singapore 8inch fab (SG8E).

Die design remains unchanged.
Electrical Wafer Sort, Assembly and Final test remain unchanged.

Why?
The strategy of the STMicroelectronics Memory division is to support our customers on product and service quality on a long-term basis. In line with this commitment, this Front-end manufacturing double source introduction will increase wafer manufacturing capacity and contribute to EEPROM business continuity security (BCP).

When?
M24128 samples are available.
M24128 qualification completed.

M24C04 and M24C02 samples available from Week 27 / 2022
M24C04 and M24C02 qualification completion Week 41 / 2022

M24C16 samples available from Week 42 / 2022
M24C16 qualification completion February / 2023

First deliveries of M24128 from SG8E will start from Week 36 / 2022
Deliveries of M24C04/02/16 will start at qualification completion.

How will the change be qualified?
This change has been qualified using the standard STMicroelectronics Corporate Procedures for Quality and Reliability.
Process technology CMOSF8H+ is qualified with driver product M24128. Other products benefit of family approach and are qualified by similarity.
Qualification Report on M24128 RERMMY2104 is available

What is the impact of the change?
- **Form:** marking change for SO8N, no change for TSSOP8 and DFN8
- **Fit:** no change
- **Function:** no change

How can the change be seen?

- DEVICE MARKING

For the **SO8N** package, the difference is visible inside the trace code (*PYWWT*) where the last digit "*T*" for the **process technology/wafer fab** identifier is "**D**" for the **additional ST Ang Mo Kio (Singapore) wafer fab**, this identifier being "T" for the current ST Rousset (France) wafer fab.

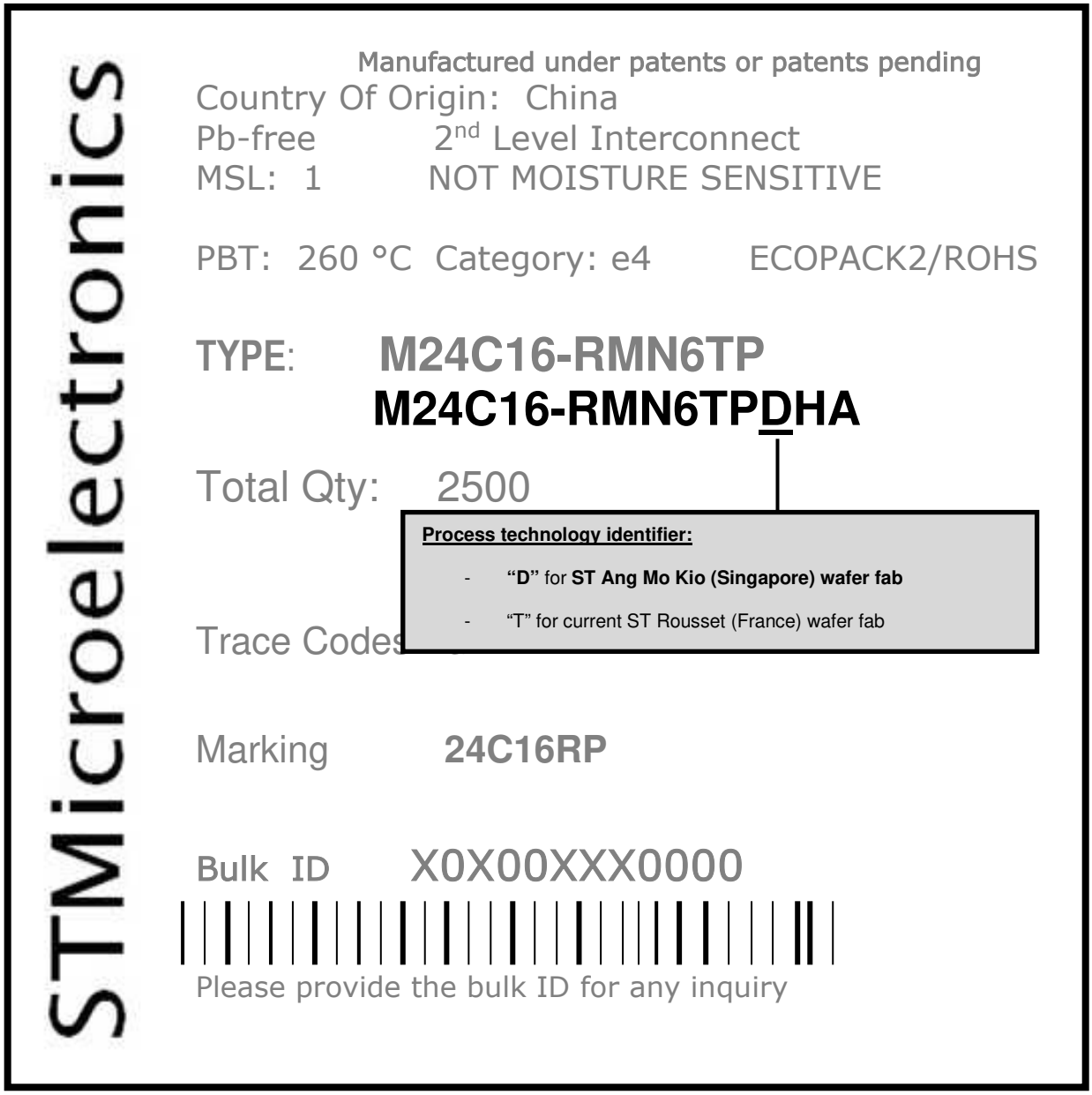
	ST Ang Mo Kio (Singapore) wafer fab	ST Rousset (France) wafer fab
SO8N Example: M24C04-RMN6TP	24C04RP *PYWW***D**	24C04RP *PYWW***T**

P = Assembly plant / country
Y = Last digit of the Year of Assembly
WW = Assembly Week code
T = Process technology code/ Wafer Fab ID

- ***BOX LABEL MARKING***

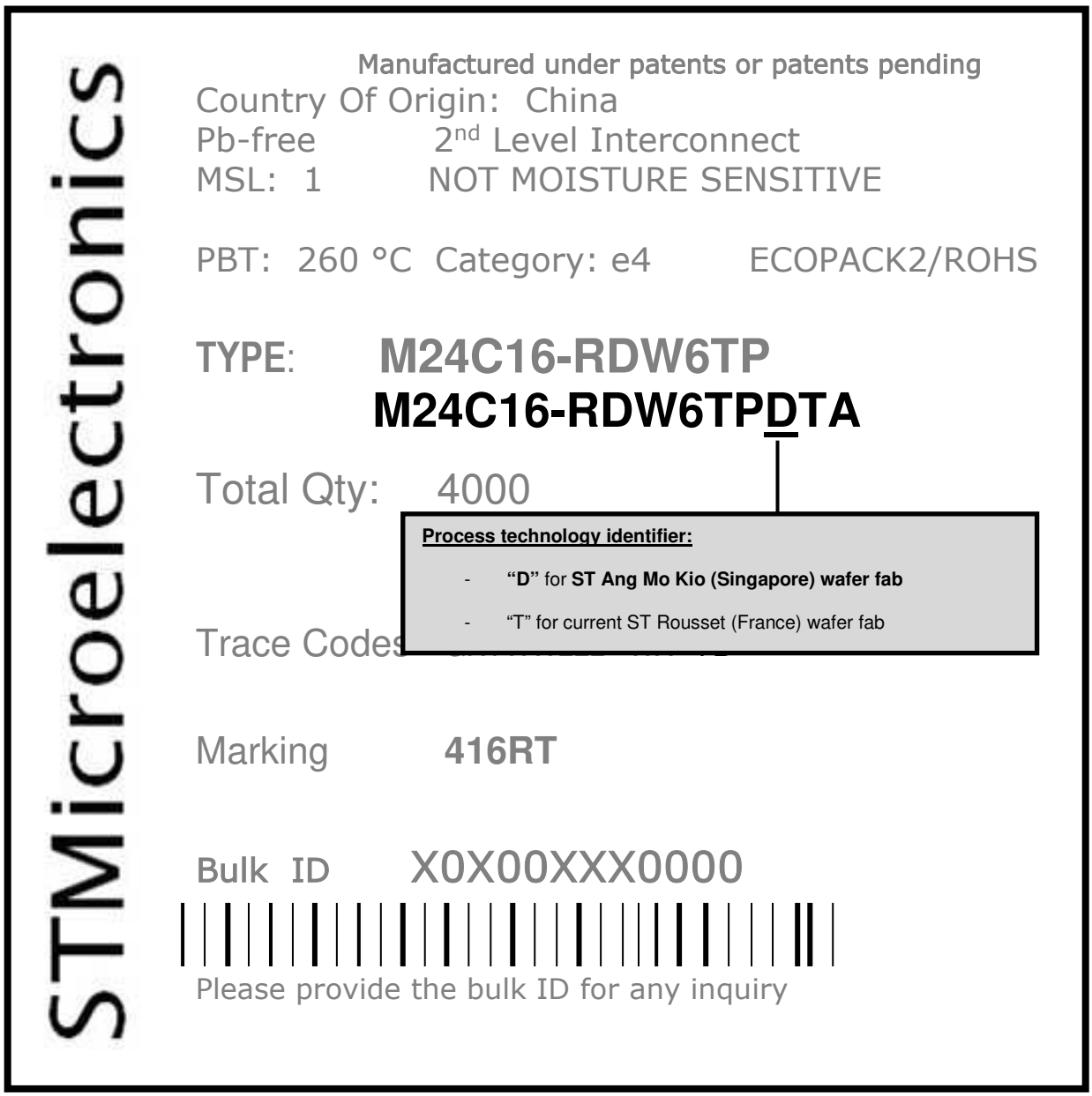
On the BOX LABEL, the difference is visible inside the **Finished Good Part Number** where the "**process technology**" identifier is "**D**" for products manufactured with CMOSF8H+ in **additional ST Ang Mo Kio (Singapore) wafer fab**, this identifier being "T" for current ST Rousset (France) wafer fab.

Example for SO8N: M24C16-RMN6TP

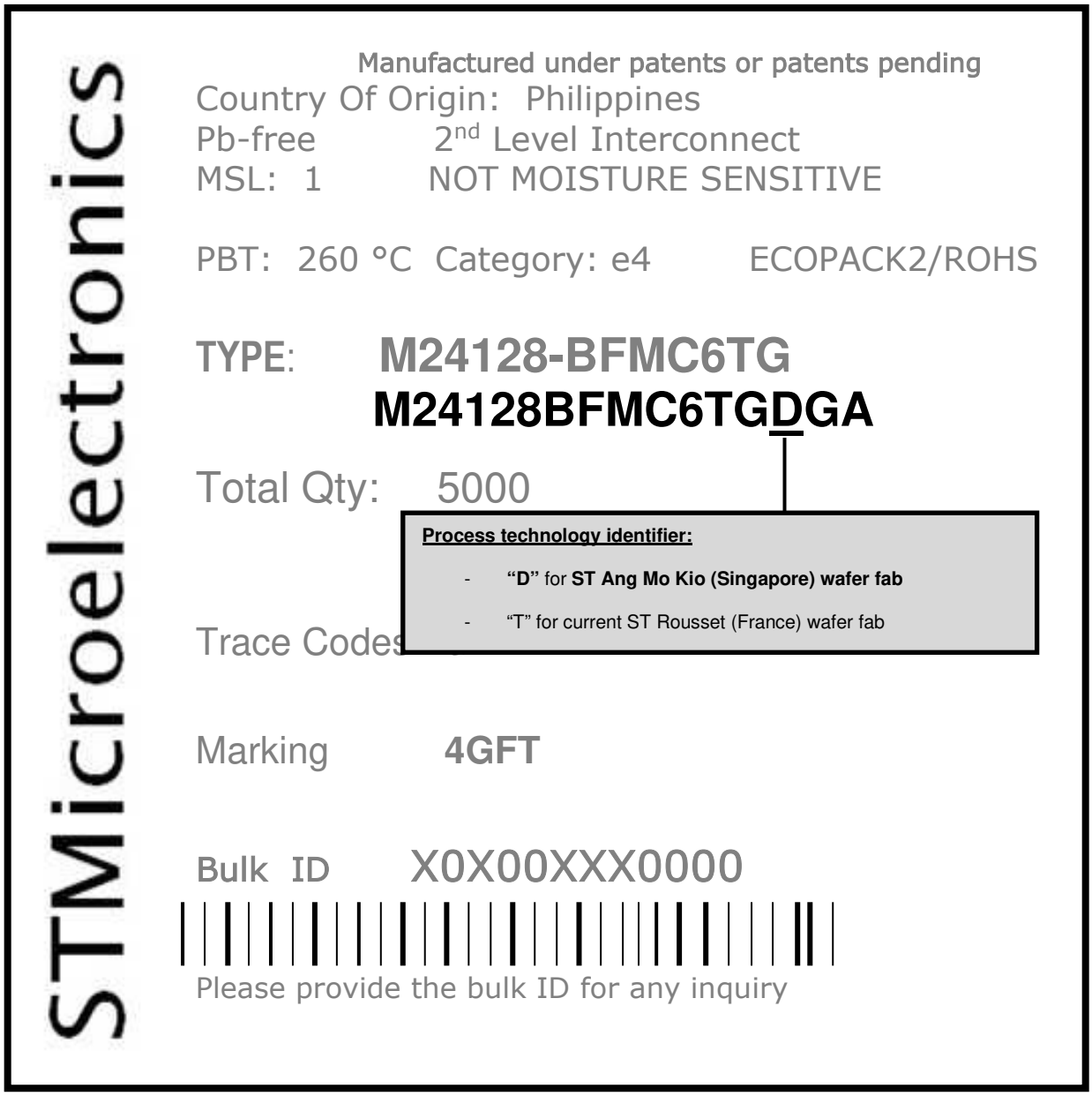


For space constraints on **TSSOP8** and **DFN8** packages, the difference is **only visible on box label**, inside the **Finished Good Part Number** as shown below:

Example for TSSOP8: M24C16-RDW6TP



Example for DFN8: M24128-BFMC6TG



Appendix A- Product Change Information

Product family / Commercial products:	Industrial grade EEPROM products manufactured with CMOSF8H+ - see Appendix B for product list
Customer(s):	All
Type of change:	Additional wafer fab
Reason for the change:	Double source
Description of the change:	Additional ST Ang Mo Kio (Singapore) wafer fab to current ST Rousset (France) wafer fab.
Forecast date of the change: (Notification to customer)	Week 23 / 2022
Forecast date of Qualification samples availability for customer(s):	As per defined in Appendix B
Qualification Report availability:	The Reliability evaluation Report RERMMY2104 is available and included inside this document. (See Appendix C)
Marking to identify the changed product:	Process technology / wafer fab identifier "**D**" on SO8N package. No marking change on TSSOP8 & DFN8.
Description of the qualification program:	Standard ST Microelectronics Corporate Procedures for Quality and Reliability
Estimated date of first shipment:	Week 36 / 2022

Appendix B: concerned Commercial Part Numbers:

Commercial product	Samples availability
M24C02-RMC6TG	Week 33 / 2022
M24C02-FMC6TG	Week 33 / 2022
M24C02-WMN6TP	Week 27 / 2022
M24C02-RMN6TP	Week 27 / 2022
M24C02-RDW6TP	Week 27 / 2022
M24C04-WMN6TP	Week 27 / 2022
M24C04-RMN6TP	Week 27 / 2022
M24C16-WMN6TP	Week 42 / 2022
M24C16-RMN6TP	Week 42 / 2022
M24C16-RDW6TP	Week 42 / 2022
M24128-BFMC6TG	Week 29 / 2022
M24128-BFMC6TG/T	Week 29 / 2022
M24128-BRMN6TP	Available
M24128-BWMN6TP	Available
M24128-BWDW6TP	Available
M24128-BRDW6TP	Available

Appendix C: Reliability Report:

See next pages

Reliability Report
RERMMY2104
FE transfer
CMOSF8H+ technology transfer from R8 to SG8E

General Information	
Commercial Product	M24128-BWMN6TP M24128-BRMN6TP
Product Line	24281D
Product Description	128 Kbit serial I2C bus EEPROM with 400 kHz clock
Package	SO8N
Silicon Technology	CMOSF8H+
Division	MEMORY

Traceability	
Diffusion Plant	ST Singapore SG8E 8"
Assembly Plant	ST Shenzhen, China

Reliability Assessment	
Pass	☒
Fail	☐

Release	Date	Author	Function
Rev 01	May 31, 2022	Eric DENIS	Division Product Quality & Reliability Engineer

DOCUMENT APPROVERS:

Name	Function	Location	Date
PAVANO Rita	Division Quality Manager	ST Rousset	May 31, 2022

RELIABILITY EVALUATION OVERVIEW

- **OBJECTIVE**

This reliability evaluation report summarizes the results of the reliability trials that were performed, in agreement with JEDEC JESD47 International Standard, to qualify the CMOSF8H+ silicon process technology in the ST SG8E 8" diffusion fab in Singapore.

The CMOSF8H+ is a known silicon process technology in the ST Rousset 8" fab, qualified for EEPROM ICs.
The qualification of CMOSF8H+ silicon process technology in ST SG8E 8" fab use M24128 as product driver.

The strategy of the STMicroelectronics Memory division is to support our customers on product and service quality on a long-term basis. In line with this commitment, this Front-end manufacturing double source introduction will increase wafer manufacturing capacity and contribute to EEPROM business continuity security (BCP).

This document serves for the qualification of the named products using the named silicon process technology in the named diffusion fab.

The voltage and temperature ranges covered by this document are:

- 1v7 to 5v5 at -40 to 85°C

- **CONCLUSION**

All reliability tests have been completed with positive results. Neither functional nor parametric rejects were
detected at final electrical testing.

Based on the overall results obtained, the CMOSF8H+ silicon process technology in the ST SG8E 8" diffusion fab in Singapore using M24128 product and assembled in SO8 package (Assy in ST Shenzhen FAB), has positively passed reliability evaluation in agreement with JEDEC JESD47 International Standard, and all products described in front page table are qualified.

TABLE OF CONTENT

1. RELIABILITY STRATEGY

This section contains a general description of the reliability evaluation strategy. The named products are qualified using the standard STMicroelectronics corporate procedures for quality and reliability.

For the new CMOSF8H+ silicon process technology in the ST SG8E 8" diffusion fab in Singapore qualification:

- Die-oriented reliability tests were run on three diffusion lots
- Package-oriented reliability tests were run on three diffusion lots

Reliability trials performed as part of this reliability evaluation are in agreement with **ST 0061692** specification
and **JEDEC JESD47 International Standard**.

2. PRODUCT OR TEST VEHICLE CHARACTERISTICS

2.1. Generalities

The M24128 device is I2C-compatible electrically erasable programmable memories (EEPROM). It is organized as 16384 × 8 bits.

I2C uses a two-wire serial interface, comprising a bi-directional data line and a clock line. The devices carry a built-in 4-bit Device Type Identifier code (1010) in accordance with the I2C bus definition.

The device behaves as a slave in the I2C protocol, with all memory operations synchronized by the serial clock. Read and Write operations are initiated by a Start condition, generated by the bus master. The Start condition is followed by a device select code and Read/Write bit (RW), terminated by an acknowledge bit.

When writing data to the memory, the device inserts an acknowledge bit during the 9th bit time, following the bus master's 8-bit transmission. When data is read by the bus master, the bus master acknowledges the receipt of the data byte in the same way. Data transfers are terminated by a Stop condition after an Ack for Write, and after a NoAck for Read.

For more details refer to the product datasheet.

2.2. Reliability testing information

Reliability Testing Information	
Reliability laboratory name / location	Grenoble Rel Lab, RCCAL, Rousset MDG Rel Lab, TPY CPA Lab
Board Level Reliability trials *(if applicable)*	
Reliability laboratory name / location	Rousset MDG Rel Lab

Note: ST is ISO 9001 certified. This induces certification of all internal and subcontractor labs. ST certification document can be downloaded under the following link: http://www.st.com/content/st_com/en/support/quality-and-reliability/certifications.html

3. TEST RESULTS SUMMARY

3.1. Product vehicles information

Product	Silicon process technology	Wafer fabrication location	Package description	Assembly plant location	Lot# / Diffusion Lot / Wafer ID
M24128	CMOSF8H	ST Singapore SG8E 8"	SO8N	ST Shenzhen	Lot 1 / C132XXX / 20

M24128	CMOSF8H	ST Singapore SG8E 8”	SO8N	ST Shenzhen	Lot 2 / C134TFN / 20
M24128	CMOSF8H	ST Singapore SG8E 8”	SO8N	ST Shenzhen	Lot 3 / C144T74 / 20

3.2. Test plan and results summary

ACCELERATED LIFETIME SIMULATION TESTS

Test code	Stress method	Stress Conditions	Lots Qty	S.S.	Total	Results/Lot Fail/S.S.	Comments: (N/A =Not Applicable)
HTOL	JESD22-A108	4 000 000 E/W cycles at 25°C + HTOL at Ta = 150°C, bias 6v0 Duration = 1000hrs ☒Testing at Room	3	77	231	Lot 1 : 0/77 Lot 2 : 0/77 Lot 3 : 0/77	
LTOL	JESD22-A108	4 000 000 E/W cycles at 25°C + LTOL at Ta = -40°C, bias 6v0 Duration = 1000hrs ☒Testing at Room	3	77	231	Lot 1 : 0/77 Lot 2 : 0/77 Lot 3 : 0/77	
PCHTDR	JESD22-A117	4 000 000 E/W cycles at 25°C + HTSL at Ta = 150°C Duration = 1000hrs ☒Testing at Room	3	77	231	Lot 1 : 0/77 Lot 2 : 0/77 Lot 3 : 0/77	
		1 200 000 E/W cycles at 85°C + HTSL at Ta = 150°C Duration = 1000hrs ☒Testing at Room	3	77	231	Lot 1 : 0/77 Lot 2 : 0/77 Lot 3 : 0/77	
LTDR	JESD22-A117	4 000 000 E/W cycles at 25 °C + HTSL at Ta = 25 °C Duration = 1000hrs ☒Testing at Room	3	77	231	Lot 1 : 0/77 Lot 2 : 0/77 Lot 3 : 0/77	

NVCE	JESD22-A117	1 200 000 E/W cycles at Ta = 85°C ☒Testing at Room	3	77	231	Lot 1 : 0/77 Lot 2 : 0/77 Lot 3 : 0/77	
		4 000 000 E/W cycles at Ta = 25°C ☒Testing at Room	3	77	231	Lot 1 : 0/77 Lot 2 : 0/77 Lot 3 : 0/77	
		4 000 000 E/W cycles at Ta = -40°C ☒Testing at Room	3	77	231	Lot 1 : 0/77 Lot 2 : 0/77 Lot 3 : 0/77	
ELFR	JESD22-A108	HTOL at Ta = 150°C, bias 6v0 Duration = 48hrs ☒Testing at Room	3	800	2400	Lot 1 : 0/800 Lot 2 : 0/800 Lot 3 : 0/800	

ACCELERATED ENVIRONMENT STRESS TESTS

Test code	Stress method	Stress Conditions	Lots Qty	S.S.	Total	Results/Lot Fail/S.S.	Comments:(N/A =Not Applicable)
PC	J-STD-020	24h bake@125°C, MSL1 (168h@85°C/85%RH) 3x Reflow simulation Peak Reflow Temp= 260°C	3	385	1155	Lot 1 : 0/385 Lot 2 : 0/385 Lot 3 : 0/385	
HAST	JESD22-A110	Ta= 130 °C, 85% RH, bias 5v6 Duration= 96hrs ☒After PC ☒Testing at Room	3	77	231	Lot 1 : 0/77 Lot 2 : 0/77 Lot 3 : 0/77	
HTSL	JESD22-A103	Ta= 150°C Duration= 1000hrs ☒After PC ☒Testing at Room	3	77	231	Lot 1 : 0/77 Lot 2 : 0/77 Lot 3 : 0/77	
TC	JESD22-A104	Ta= -65 °C / 150 °C Cycles= 1000 ☒After PC ☒Testing at Room	3	77	231	Lot 1 : 0/77 Lot 2 : 0/77 Lot 3 : 0/77	
THB	JESD22-A101	Ta= 85 °C, 85% RH, bias 5v6 Duration= 1000hrs ☒After PC ☒Testing at Room	3	77	231	Lot 1 : 0/77 Lot 2 : 0/77 Lot 3 : 0/77	
UHAST	JESD22-A118	Ta= 130 °C, 85% RH, No bias Duration= 96hrs ☒After PC ☒Testing at Room	3	77	231	Lot 1 : 0/77 Lot 2 : 0/77 Lot 3 : 0/77	

Electrical Verification Tests

Test code	Stress method	Stress Conditions	Lots Qty	S.S.	Total	Results/Lot Fail/S.S.	Comments:(N/A =Not Applicable)
ESD CDM	ANSI/ESDA/ JEDEC JS-002	Ta= 25°C, target CDM = +/-500V ☒Testing at Room	3	18	54	Lot 1 : > 1500V Lot 2 : > 1500V Lot 3 : > 1500V	Class C3

ESD HBM	ANSI/ESDA/ JEDEC JS-001	Ta= 25°C, target HBM = /- 2kV ☒Testing at Room	3	60	180	Lot 1: > 2000V Lot 2: > 2000V Lot 3: > 2000V	Class 3A
LU	JESD78	Ta= 150°C, current injection +/- 200mA ☒Testing at Room	3	6	18	Lot 1 : 0/6 Lot 2 : 0/6 Lot 3 : 0/6	Class II level A

Note: Test method revision reference is the one active at the date of reliability trial execution.

4. APPLICABLE AND REFERENCE DOCUMENTS

Reference	Short description
JESD47	Stress-Test-Driven Qualification of Integrated Circuits
SOP2.4.4	Record Management Procedure
SOP2.6.2	Internal Change Management
SOP2.6.7	Finished Good Maturity Management
SOP2.6.9	Package & Process Maturity Management in BE
SOP2.6.11	Program Management for Product Development
SOP2.6.17	Management of Manufacturing Transfers
SOP2.6.19	Front-End Technology Platform Development and Qualification
DMS 0061692	Reliability Tests and Criteria for Product Qualification
J-STD-020	Moisture/Reflow Sensitivity Classification for Nonhermetic Surface Mount Devices
JESD22-A101	Steady state temperature humidity bias life test
JESD22-A103	High temperature storage life
JESD22-A104	Temperature cycling
JESD22-A108	Temperature, bias, and operating life
JESD22-A110	Highly Accelerated Temperature and Humidity Stress Test
JESD22-A117	Electrically Erasable Programmable ROM (EEPROM) Program / Erase Endurance and Data Retention Stress Test
JESD22-A118	Accelerated Moisture Resistance - Unbiased HAST
JS-001	Human Body Model (HBM)
JS-002	Charged Device Model (CDM)
JESD78	Latch-Up

5. GLOSSARY

CDM	Electrostatic Discharge – Charged Device Model
ELFR	Early Life Failure Rate
HAST	Highly Accelerated Stress Test
HBM	Electrostatic Discharge - Human Body Model
HTOL	High Temperature Operating Life
HTSL	High Temperature Storage Life
LTDR	Nonvolatile Memory Low Temperature Data Retention and Read Disturb
LTOL	Low Temperature Operating Life
LU	Latch-Up
NVCE	Nonvolatile Memory Cycling Endurance
PC	Preconditioning
PCHTDR	Nonvolatile Memory Post-Cycling High Temperature Data Retention
TC	Temperature Cycling
THB	Temperature Humidity Bias
UHAST	Unbiased Highly Accelerated Stress Test

6. REVISION HISTORY

Release	Date	Description
Rev 01	May 31st, 2022	Initial release

TERMS OF USE

BY ACCEPTING THIS REPORT, YOU AGREE TO THE FOLLOWING TERMS OF USE:

This Reliability Report (the "Report") and all information contained herein is the property of STMicroelectronics ("ST") and is provided solely for the purpose of obtaining general information relating to an ST product. Accordingly, you hereby agree to make use of this Report solely for the purpose of obtaining general information relating to the ST product. You further acknowledge and agree that this Report may not be used in or in connection with any legal or administrative proceeding in any court, arbitration, agency, commission or other tribunal or in connection with any action, cause of action, litigation, claim, allegation, demand or dispute of any kind. You further acknowledge and agree that this Report shall not be construed as an admission, acknowledgement or evidence of any kind, including, without limitation, as to the liability, fault or responsibility whatsoever of ST or any of its affiliates, or as to the accuracy or validity of the information contained herein, or concerning any alleged product issue, failure, or defect. ST does not promise that this Report is accurate or error free and specifically disclaims all warranties, express or implied, as to the accuracy of the information contained herein. Accordingly, you agree that in no event will ST or its affiliates be liable to you for any direct, indirect, consequential, exemplary, incidental, punitive, or other damages, including lost profits, arising from or relating to your reliance upon or use of this Report. You further acknowledge and agree that the use of this Report in violation of these Terms of Use would cause immediate and irreparable harm to ST which could not adequately be remedied by damages. You therefore agree that injunctive relief is an appropriate remedy to enforce these Terms of Use.

Disclosure of this document to any non-authorized party must be previously authorized by ST only under the provision of a proper confidentiality contractual arrangement executed between ST and you and must be treated as strictly confidential.
At all times you will comply with the following rules:

- Do not copy or reproduce all or part of this document
- Keep this document locked away
- Further copies can be provided on a "need to know basis", Please contact your local ST Sales Office or document writer

Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST's terms and conditions of sale in place at the time of order acknowledgement, including, without limitation, the warranty provisions thereunder.

In that respect please note that ST products are not designed for use in some specific applications or environments described in above mentioned terms and conditions.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of Purchasers' products.

Information furnished is believed to be accurate and reliable. However, ST assumes no responsibility for the consequences of use of such information nor for any infringement of patents or other rights of third parties which may result from its use. No license, express or implied, to any intellectual property right is granted by ST herein.

ST and ST logo are trademarks of ST. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously contained in any prior version of this document.

Document Revision History

Date	Rev.	Description of the Revision
Apr. 04, 2022	1.00	Christian POLI - First draft creation

Source Documents & Reference Documents

Source document Title	Rev.:	Date: